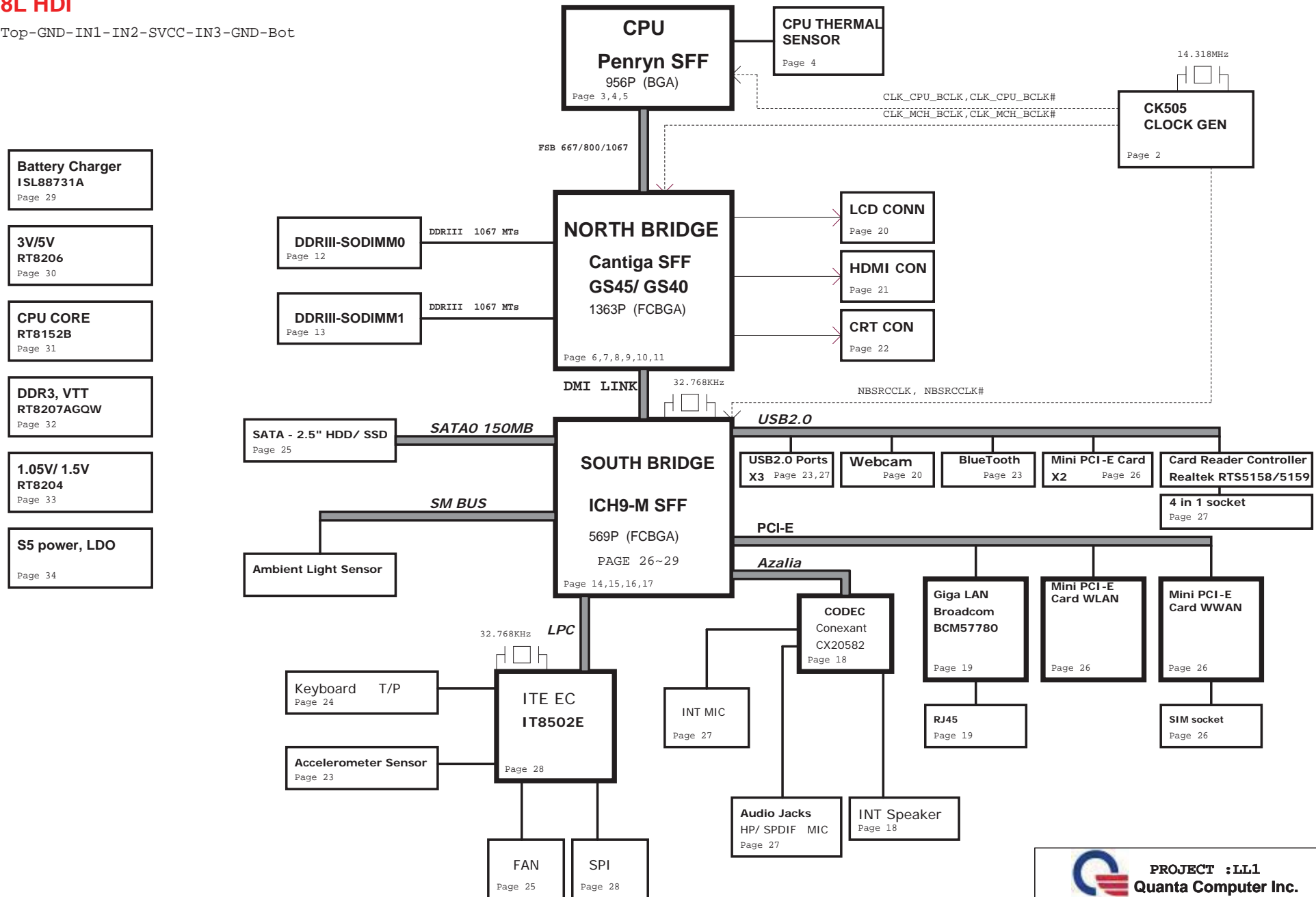
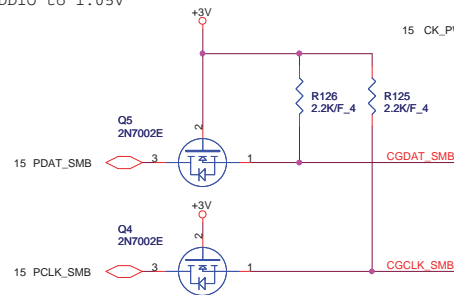
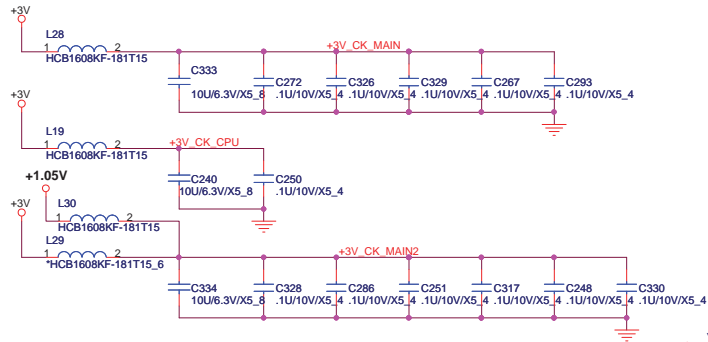


Crimea, LL1 BLOCK DIAGRAM

01

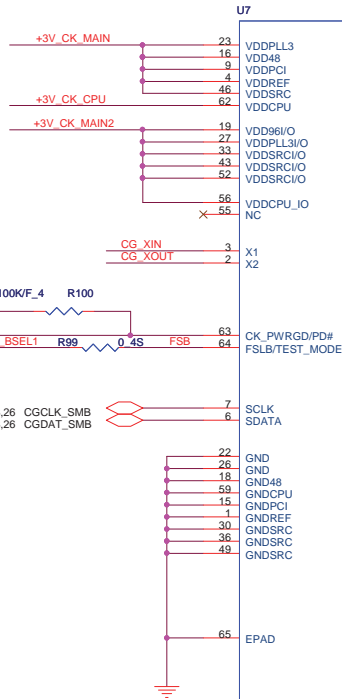




TME=High
OC of CPU and SRC are not allowed.

27M_SEL= LOW UMA

0211 Disable ITP.

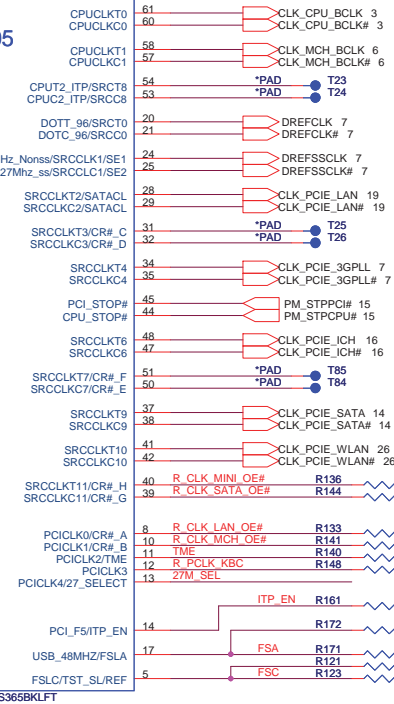


CK505

CLKREQ SRC Port

CR#_B	SRC 1,4	CLK_MCH_OE#	SRC4
CR#_A	SRC 0,2	CLK_LAN_OE#	SRC2
CR#_G	SRC 9	CLK_SATA_OE#	SRC9
CR#_H	SRC 10	CLK_MINI_OE#	SRC10

0218 Connect WLAN OE#



CPU Differential Host Clock

NB Differential Host Clock

NB Display PLLA Differential Clock

NB Display PLLB Differential Clock

PCI-E LAN

0220 Change to SRC1 for SS.

NB Differential PCI Express based Graphics/DMI Clock

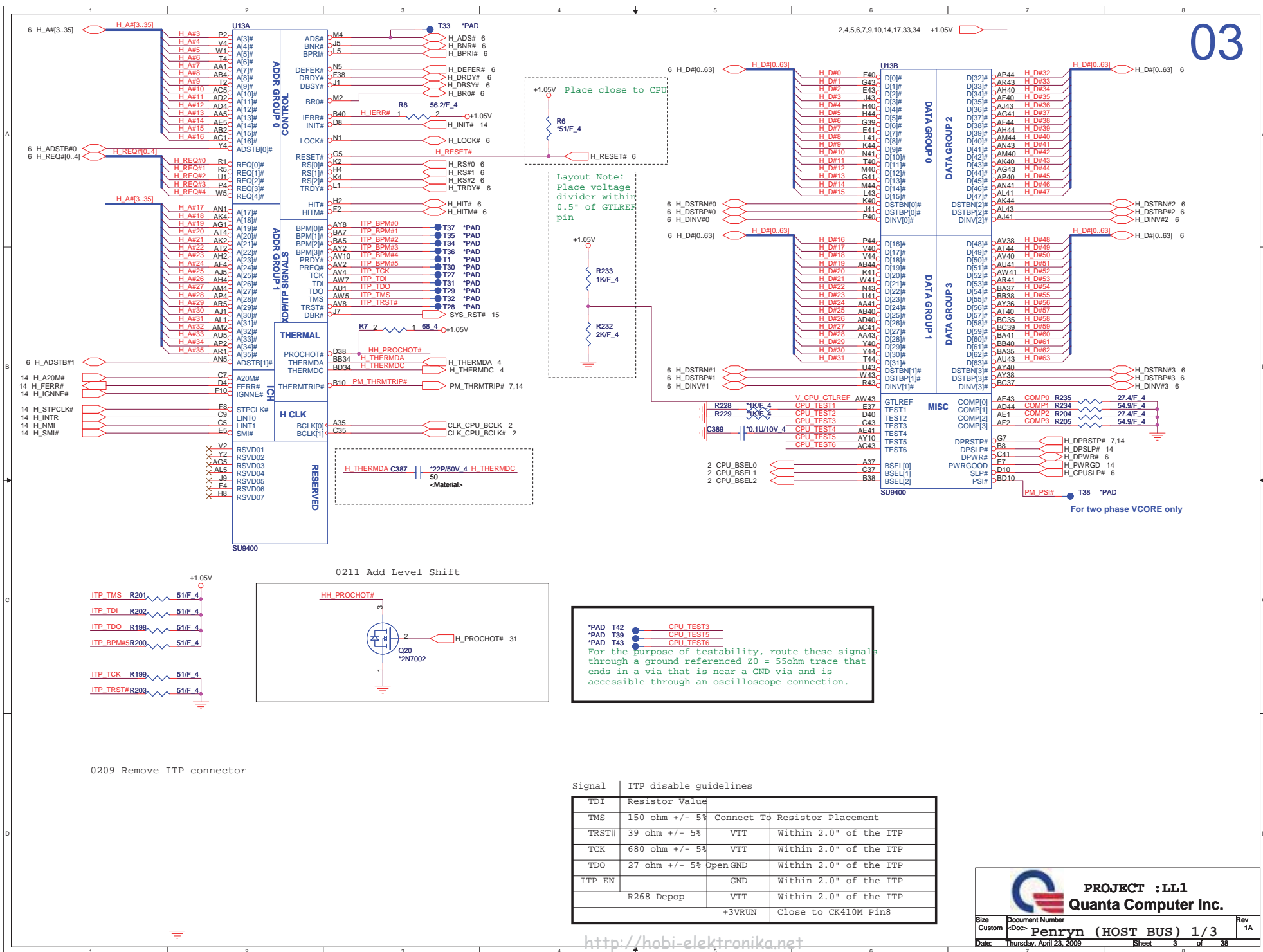
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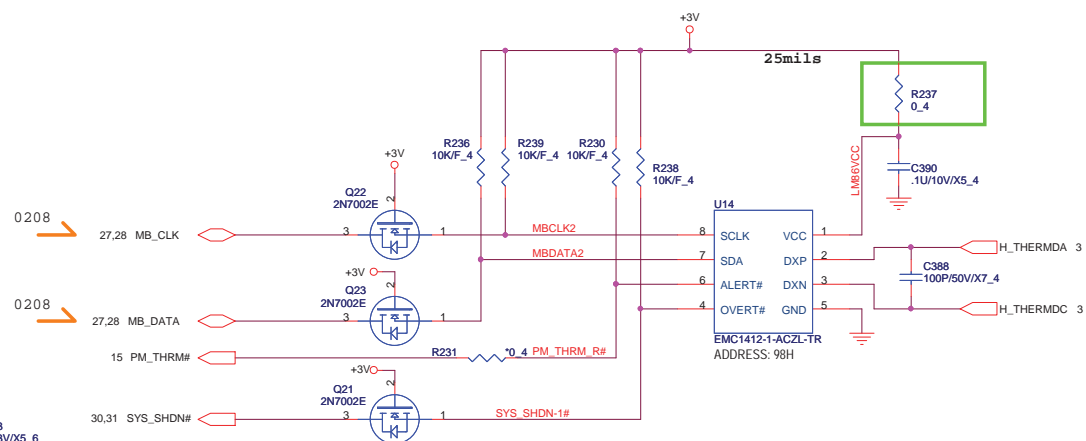
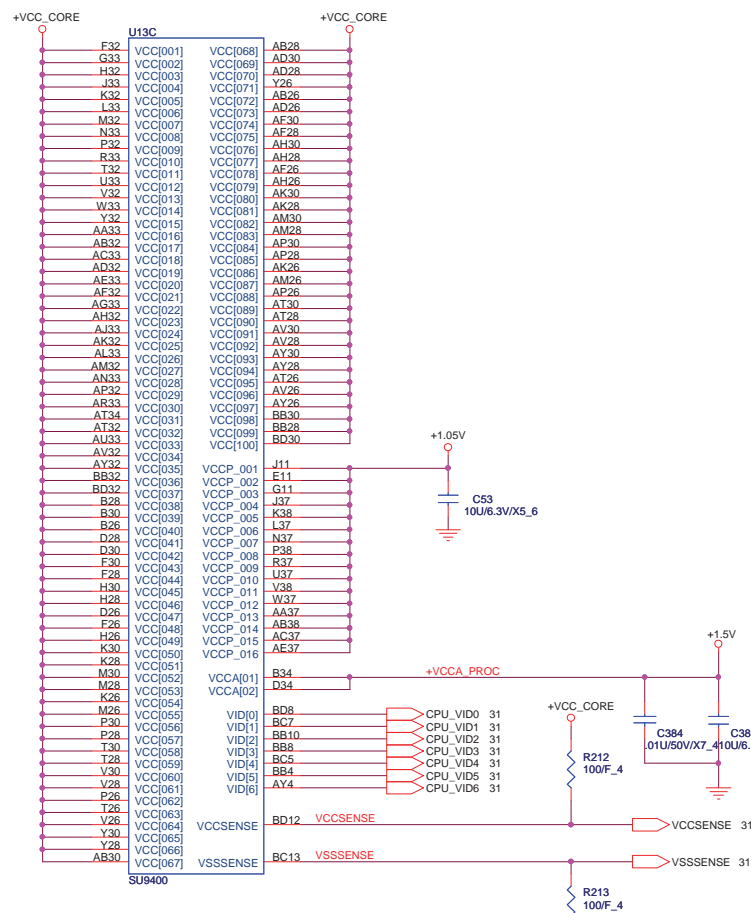
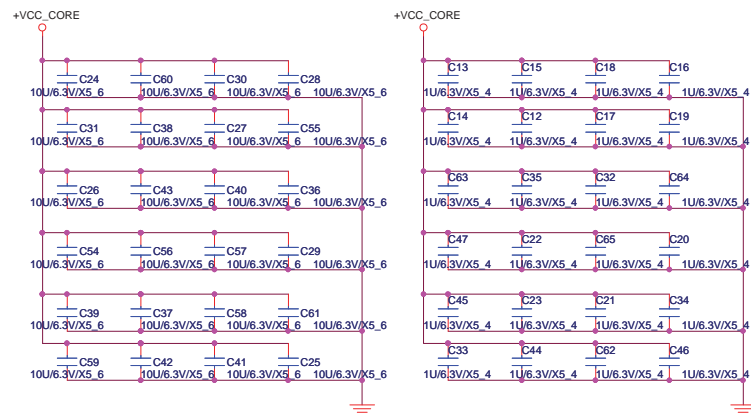
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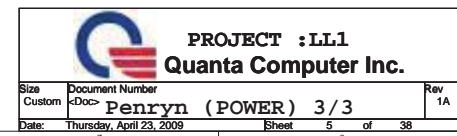
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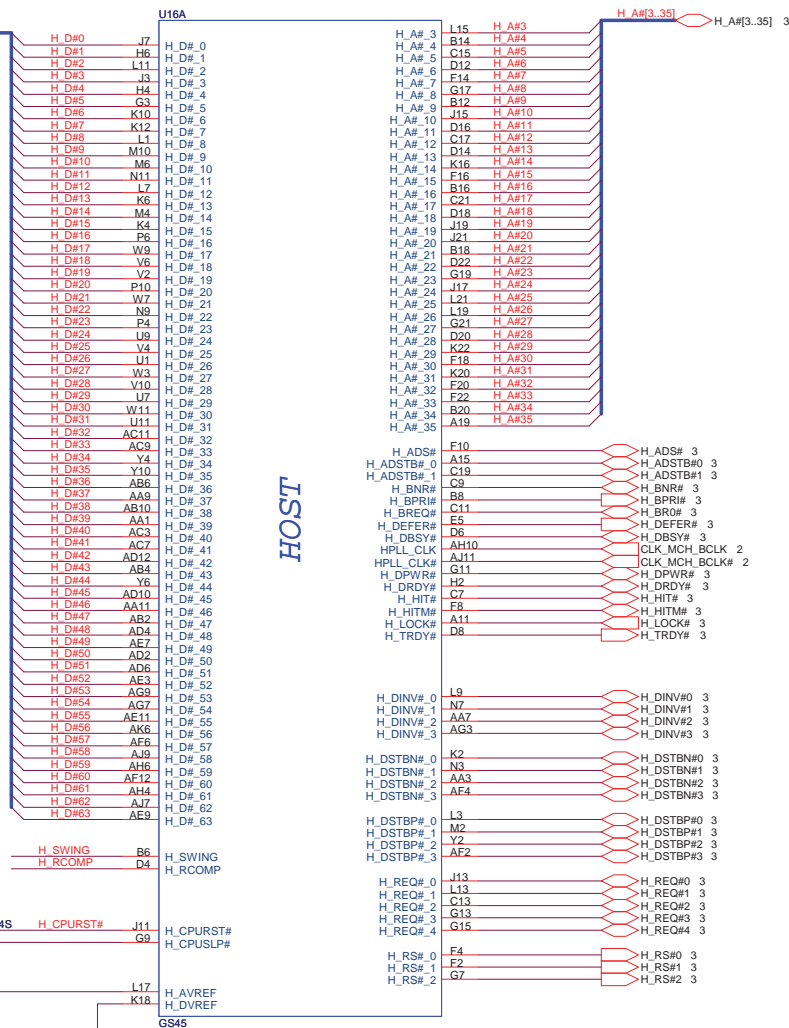
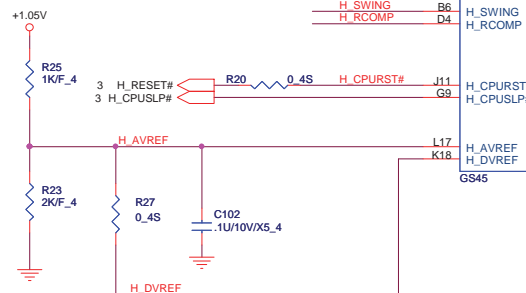
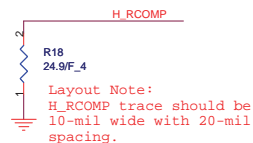
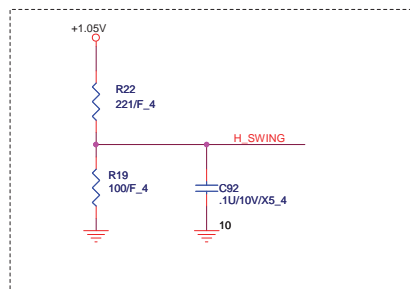
WLAN











12 DDR_A_D[0..63]

DDR A D0 AP46
DDR A D1 AU47
DDR A D2 AT46
DDR A D3 AU49
DDR A D4 AR45
DDR A D5 AN49
DDR A D6 AV50
DDR A D7 AF50
DDR A D8 AW47
DDR A D9 BD50
DDR A D10 AW49
DDR A D11 BA49
DDR A D12 BC49
DDR A D13 AV42
DDR A D14 BA47
DDR A D15 AY50
DDR A D16 BF46
DDR A D17 BC47
DDR A D18 BF50
DDR A D19 BF48
DDR A D20 BC43
DDR A D21 BE49
DDR A D22 BA43
DDR A D23 BE47
DDR A D24 BF42
DDR A D25 BC38
DDR A D26 BE44
DDR A D27 BF40
DDR A D28 BB40
DDR A D29 BE43
DDR A D30 BF38
DDR A D31 BE41
DDR A D32 BA15
DDR A D33 BE11
DDR A D34 BE15
DDR A D35 BF14
DDR A D36 BB14
DDR A D37 BC15
DDR A D38 BE13
DDR A D39 BF16
DDR A D40 BF10
DDR A D41 BC11
DDR A D42 BF8
DDR A D43 BG7
DDR A D44 BC7
DDR A D45 BC9
DDR A D46 BD6
DDR A D47 BF12
DDR A D48 AV6
DDR A D49 BB6
DDR A D50 AW7
DDR A D51 AY6
DDR A D52 AT10
DDR A D53 AW11
DDR A D54 AU11
DDR A D55 AR9
DDR A D56 AR11
DDR A D57 AT6
DDR A D58 AP6
DDR A D59 AL7
DDR A D60 AR7
DDR A D61 AT12
DDR A D62 AM6
DDR A D63 AU7

U16D

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2

SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BC21 DDR A BS0
BJ21 DDR A BS1
BJ41 DDR A BS2
BH22 DDR A RAS#
BK20 DDR A CAS#
BL15 DDR A WE#

AT50 DDR A DM0
BB50 DDR A DM1
BB46 DDR A DM2
BE39 DDR A DM3
BB12 DDR A DM4
BE7 DDR A DM5
AV10 DDR A DM6
AR9 DDR A DM7

AR47 DDR A DQS0
BA45 DDR A DQS1
BE45 DDR A DQS2
BC41 DDR A DQS3
BC13 DDR A DQS4
BB10 DDR A DQS5
BA7 DDR A DQS6
AN7 DDR A DQS7

AR49 DDR A DQS#0
AW45 DDR A DQS#1
BC45 DDR A DQS#2
BA41 DDR A DQS#3
BA13 DDR A DQS#4
BA11 DDR A DQS#5
BA9 DDR A DQS#6
AN9 DDR A DQS#7

BC23 DDR A MA0
BE22 DDR A MA1
BE31 DDR A MA2
BC31 DDR A MA3
BH26 DDR A MA4
BJ35 DDR A MA5
BB34 DDR A MA6
BH32 DDR A MA7
BB26 DDR A MA8
BF32 DDR A MA9
BA21 DDR A MA10
BG25 DDR A MA11
BH34 DDR A MA12
BH18 DDR A MA13
BE25 DDR A MA14

13 DDR_B_D[0..63]

DDR B D0 AP54
DDR B D1 AM52
DDR B D2 AR55
DDR B D3 AV54
DDR B D4 AM54
DDR B D5 AN53
DDR B D6 AT52
DDR B D7 AU53
DDR B D8 AW53
DDR B D9 AY52
DDR B D10 BB52
DDR B D11 BC53
DDR B D12 AV52
DDR B D13 AV52
DDR B D14 BD52
DDR B D15 BC55
DDR B D16 BF54
DDR B D17 BE51
DDR B D18 BH48
DDR B D19 BK48
DDR B D20 BE53
DDR B D21 BH52
DDR B D22 BK46
DDR B D23 BJ47
DDR B D24 BL45
DDR B D25 BL45
DDR B D26 BL41
DDR B D27 BH44
DDR B D28 BH46
DDR B D29 BK44
DDR B D30 BK40
DDR B D31 BJ39
DDR B D32 BK10
DDR B D33 BH10
DDR B D34 BK6
DDR B D35 BH6
DDR B D36 BJ9
DDR B D37 BL11
DDR B D38 BG5
DDR B D39 BJ5
DDR B D40 BG3
DDR B D41 BF4
DDR B D42 BD4
DDR B D43 BA3
DDR B D44 BE5
DDR B D45 BF2
DDR B D46 BB4
DDR B D47 AY4
DDR B D48 BA1
DDR B D49 AF2
DDR B D50 AU11
DDR B D51 AT2
DDR B D52 AT4
DDR B D53 AV4
DDR B D54 AU3
DDR B D55 AR3
DDR B D56 AN1
DDR B D57 AP4
DDR B D58 AL3
DDR B D59 AI1
DDR B D60 AK4
DDR B D61 AM4
DDR B D62 AH2
DDR B D63 AK2

U16E

DDR SYSTEM MEMORY B

SB_BS_0
SB_BS_1
SB_BS_2

SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BJ13 DDR B BS0
BK12 DDR B BS1
BK38 DDR B BS2
BE21 DDR B RAS#
BH14 DDR B CAS#
BK14 DDR B WE#

AP52 DDR B DM0
BJ54 DDR B DM1
BJ49 DDR B DM2
BJ43 DDR B DM3
BH12 DDR B DM4
BD2 DDR B DM5
AY2 DDR B DM6
AJ3 DDR B DM7

AR53 DDR B DQS0
BA53 DDR B DQS1
BH50 DDR B DQS2
BK42 DDR B DQS3
BH6 DDR B DQS4
BB2 DDR B DQS5
AV2 DDR B DQS6
AM2 DDR B DQS7

AT54 DDR B DQS#0
BB54 DDR B DQS#1
BJ51 DDR B DQS#2
BH42 DDR B DQS#3
BK8 DDR B DQS#4
BC3 DDR B DQS#5
AW3 DDR B DQS#6
AN3 DDR B DQS#7

BJ15 DDR B MA0
BJ33 DDR B MA1
BH24 DDR B MA2
BA17 DDR B MA3
BF36 DDR B MA4
BH36 DDR B MA5
BF34 DDR B MA6
BK34 DDR B MA7
BJ37 DDR B MA8
BH40 DDR B MA9
BH16 DDR B MA10
BK36 DDR B MA11
BH38 DDR B MA12
BJ11 DDR B MA13
BL37 DDR B MA14

GS45

GS45

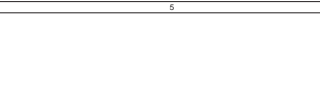
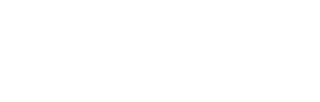
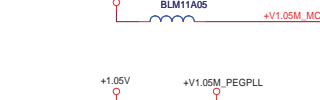
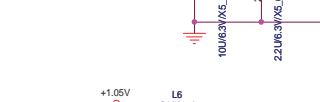
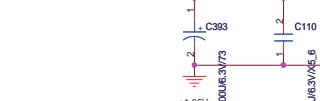
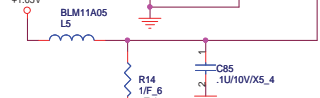
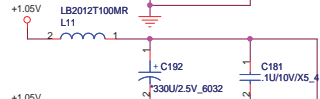
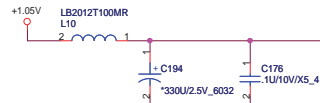


PROJECT :LL1
Quanta Computer Inc.

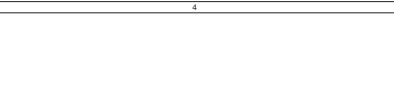
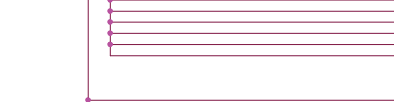
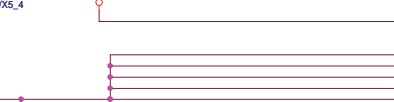
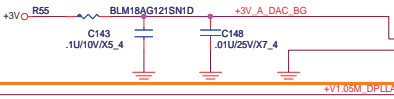
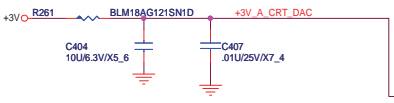
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Date: Thursday, April 23, 2009 Sheet 8 of 38

VCCA_DPLLA+VCCA_DPLLB=64.8mA



0218 Correct as Design Guide



U16H

VCCA_CRT_DAC

VCCA_DAC_BG

VCCA_DPLLA

VCCA_DPLLB

VCCA_HPLL

VCCA_MPLL

VCCA_LVDS1

VCCA_LVDS2

VSSA_LVDS

VCCA_PEG_BG

VCCA_PEG_PL

VCCA_SM_1

VCCA_SM_2

VCCA_SM_3

VCCA_SM_4

VCCA_SM_5

VCCA_SM_6

VCCA_SM_7

VCCA_SM_8

VCCA_SM_9

VCCA_SM_10

VCCA_SM_11

VCCA_SM_12

VCCA_SM_13

VCCA_SM_14

VCCA_SM_15

VCCA_SM_16

VCCA_SM_17

VCCA_SM_NCTF_1

VCCA_SM_NCTF_2

VCCA_SM_NCTF_3

VCCA_SM_NCTF_4

VCCA_SM_NCTF_5

VCCA_SM_NCTF_6

VCCA_SM_NCTF_7

VCCA_SM_NCTF_8

VCCA_SM_NCTF_9

VCCA_SM_NCTF_10

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VCCA_SM_NCTF_15

VCCA_SM_NCTF_16

VCCA_SM_NCTF_17

VCCA_SM_NCTF_18

VCCA_SM_NCTF_19

VCCA_SM_NCTF_20

VCCA_SM_NCTF_21

VCCA_SM_NCTF_22

VCCA_SM_NCTF_23

VCCA_SM_NCTF_24

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VCCA_SM_NCTF_103

VCCA_SM_NCTF_104

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VCCA_SM_NCTF_106

VCCA_SM_NCTF_107

VCCA_SM_NCTF_108

VCCA_SM_NCTF_109

VCCA_SM_NCTF_110

VCCA_SM_NCTF_111

VCCA_SM_NCTF_112

VCCA_SM_NCTF_113

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VCCA_SM_NCTF_175

VCCA_SM_NCTF_176

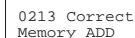
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VCCA_SM_NCTF_178

VCCA_SM_NCTF_179

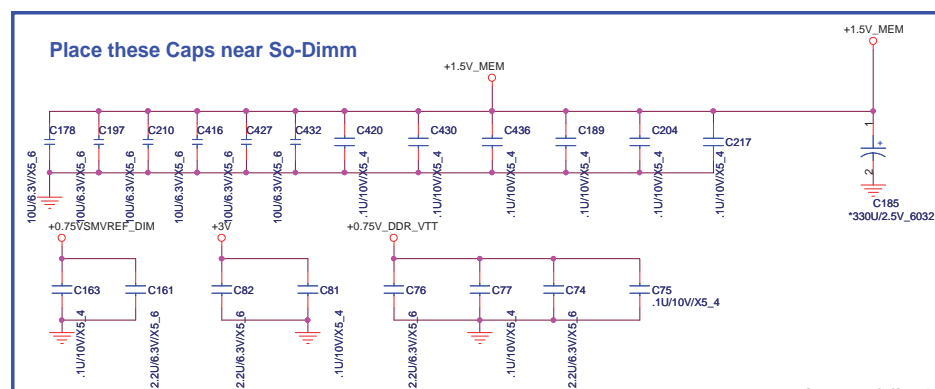
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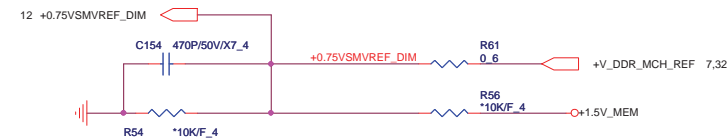


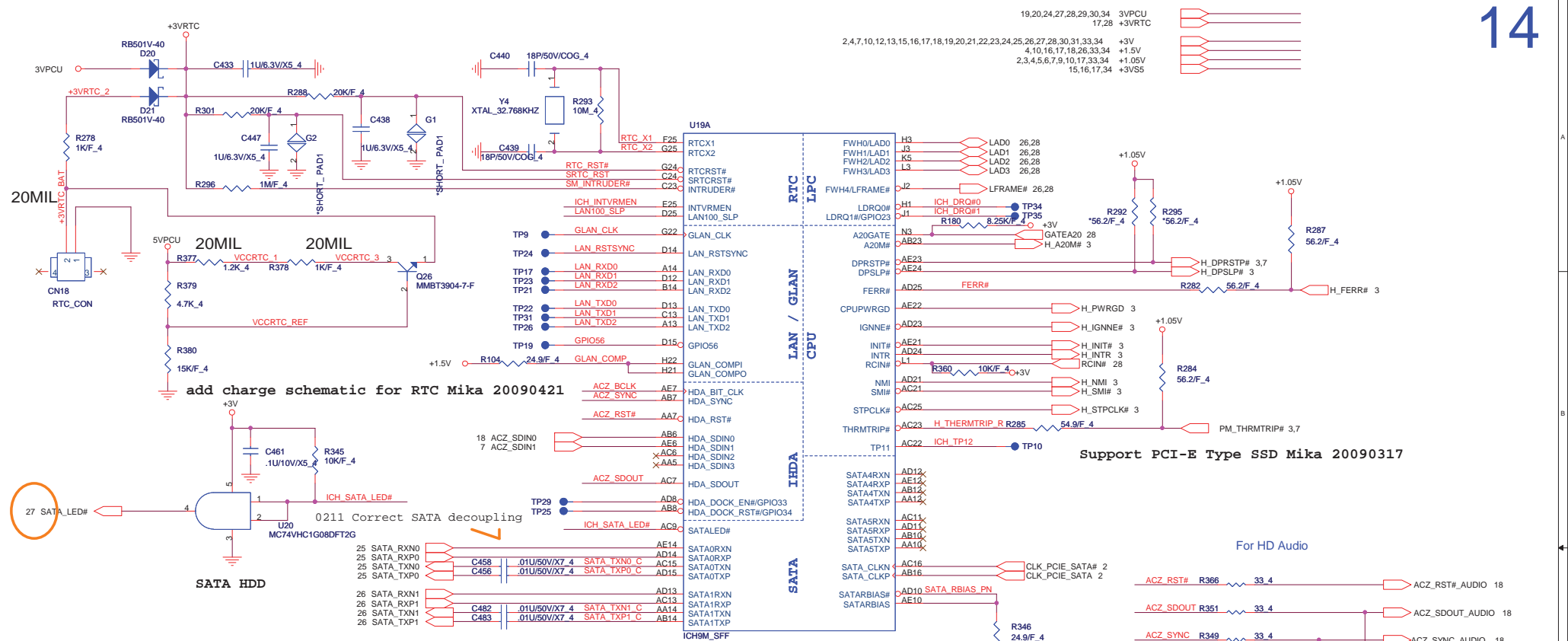


PC2100 DDR3 SDRAM SO-DIMM
(204P)

CONN_DDR3_RVS
H5.2. DDR3 REVERSE







PCI-E Type SSD change to SATA1 Mika 20090320

SB Strap

ICH9-M Internal VR
Enable strap
(Internal VR for
Vccsusi_05, Vccsusi_1_5
and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for
VccLAN1_05 and
VccCL1_05)

INTVRMEN
Low = Internal VR disable
High = Internal VR enable(Default)

LAN100_SLP
Low = Internal VR disable
High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

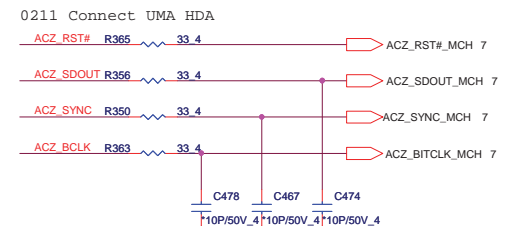
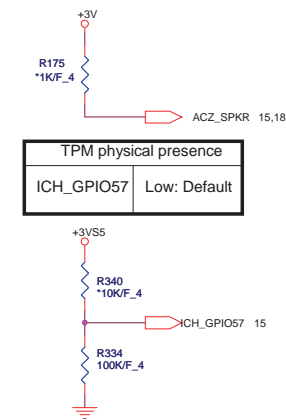
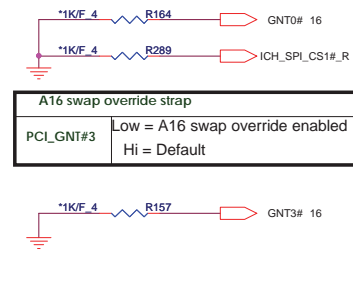
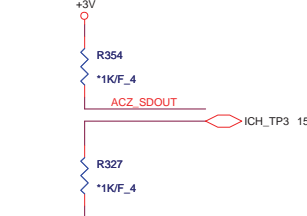
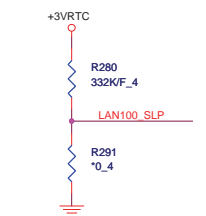
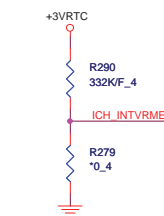
STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

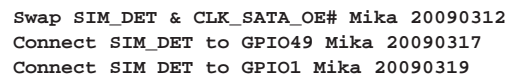
No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

TPM physical presence	
ICH_GPIO57	Low: Default



PROJECT : ILL1
Quanta Computer Inc.

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Custom	ICH9-M A (CPU, SATA, IDE)	1A
Date	Thursday, April 23, 2009	Sheet 14 of 38



0207 WWAN

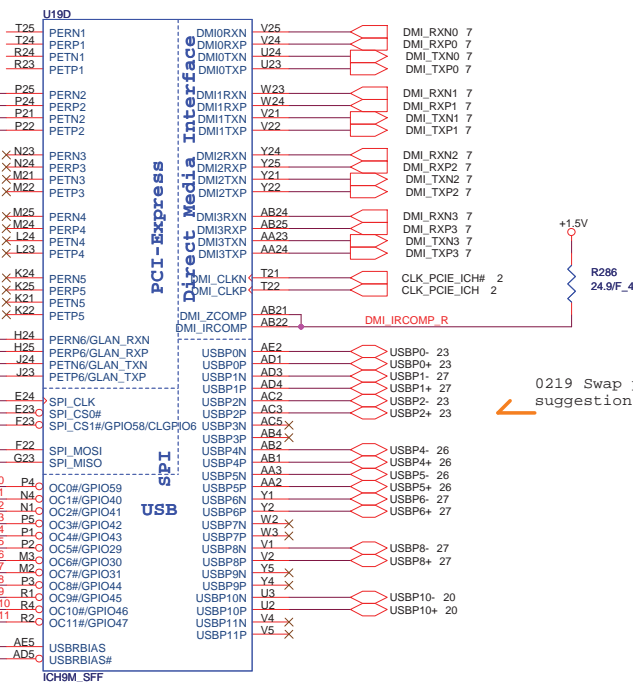
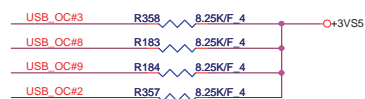
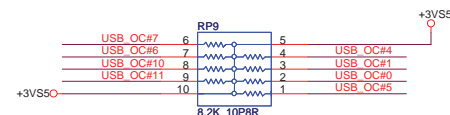
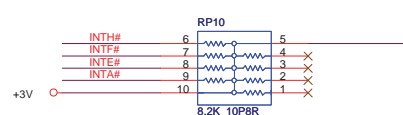
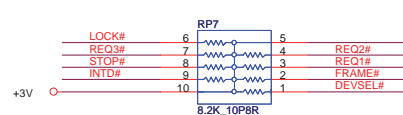
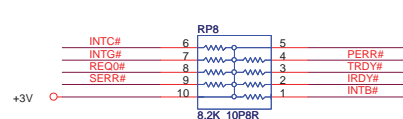
Del PCI-E interface (WWAN use USB type) Mika 20090317

Change WLAN to PCI-E-2 Mika 20090318

LAN



0219

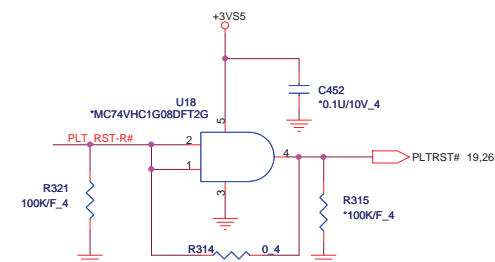


0219 Swap per SW
suggestion.

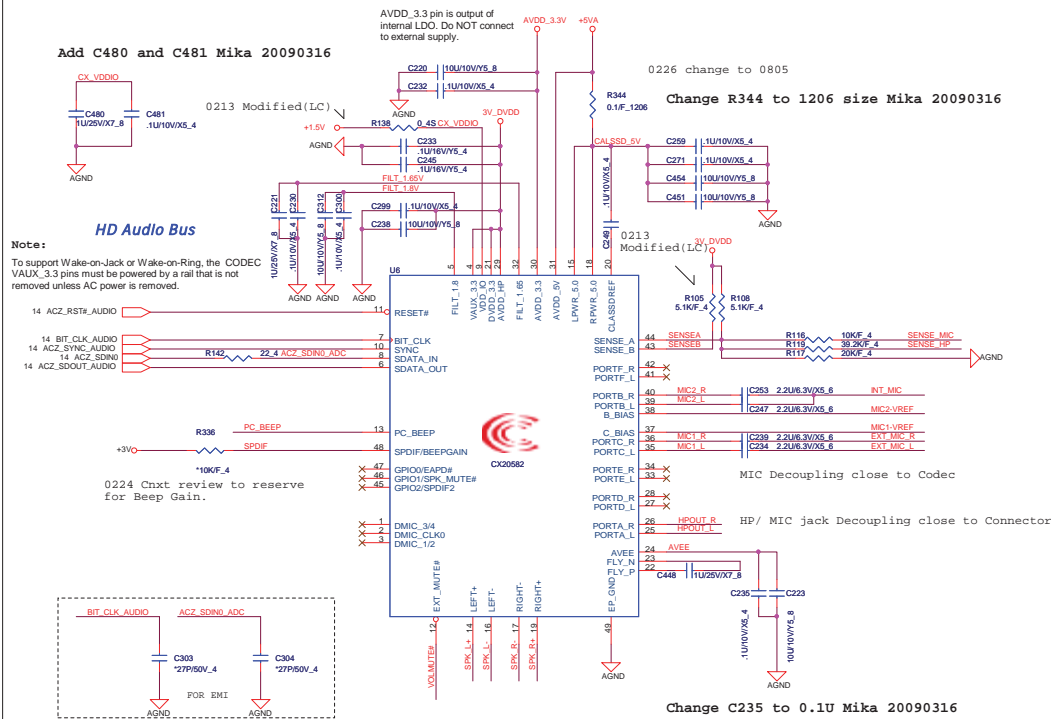
USB port

Assignment function

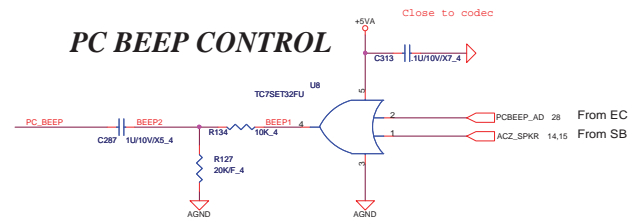
USB0	USB Connector onboard
USB1	USB Connector on function board
USB2	BLUETOOTH
USB3	X
USB4	Mini PCI E
USB5	Mini PCI E
USB6	USB Connector on function board
USB7	X
USB8	USB Card Reader on function board
USB9	X
USB10	CCD
USB11	X





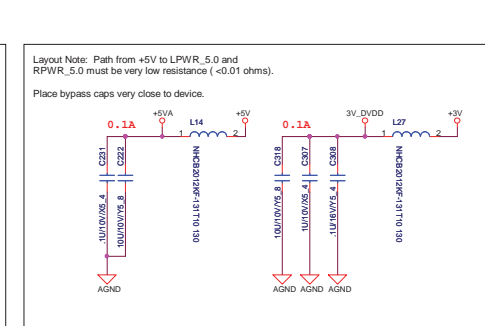
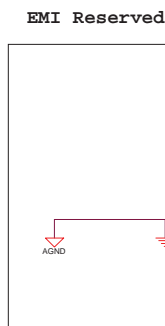
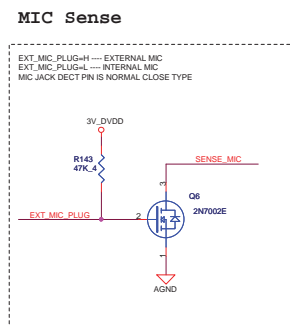
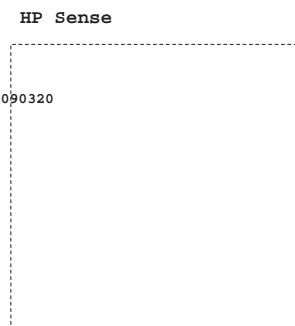
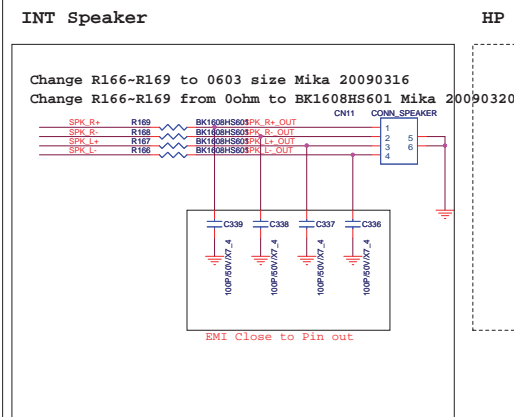


PC BEEP CONTROL

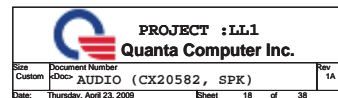


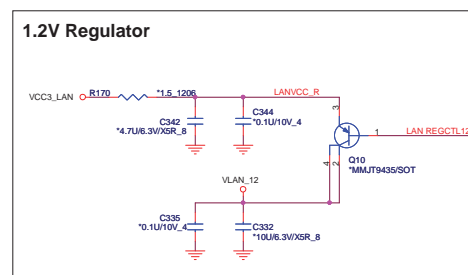
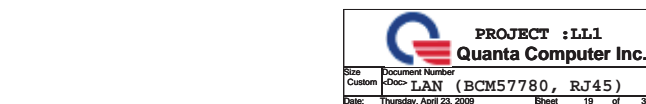
Del R156 and Q8 then short Volmute# directly Mika 20090318

```
Change PC_BEEP voltage level to 1/10 Mika 20090319
Change PC_BEEP voltage level to 2/3 Mika 20090421
```

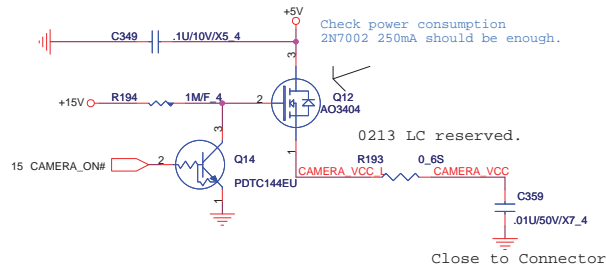


Del R94,R163 to short AGND and GND directly Mika 20090316



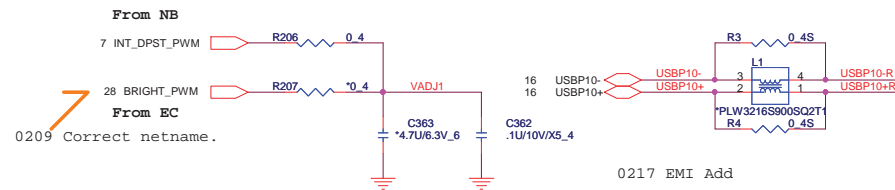
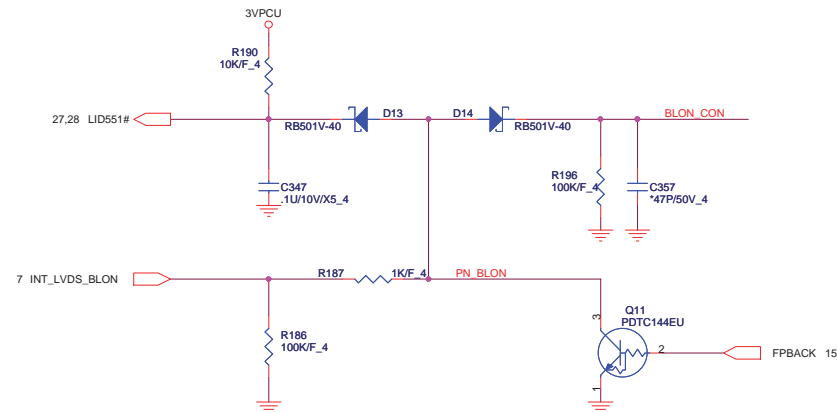


CCD POWER CONTROL

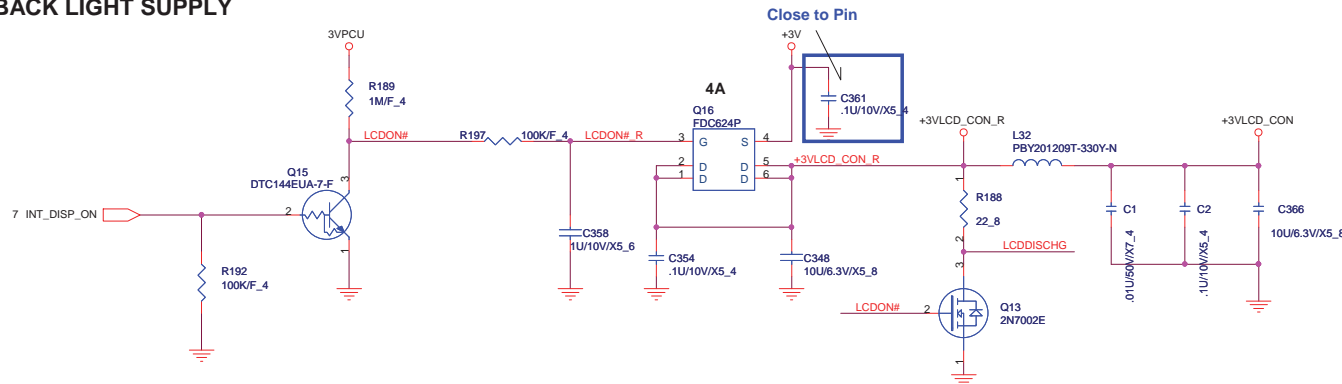


SUPPORT 13.3" LED TYPE LCD

BACK LIGHT CONTROL

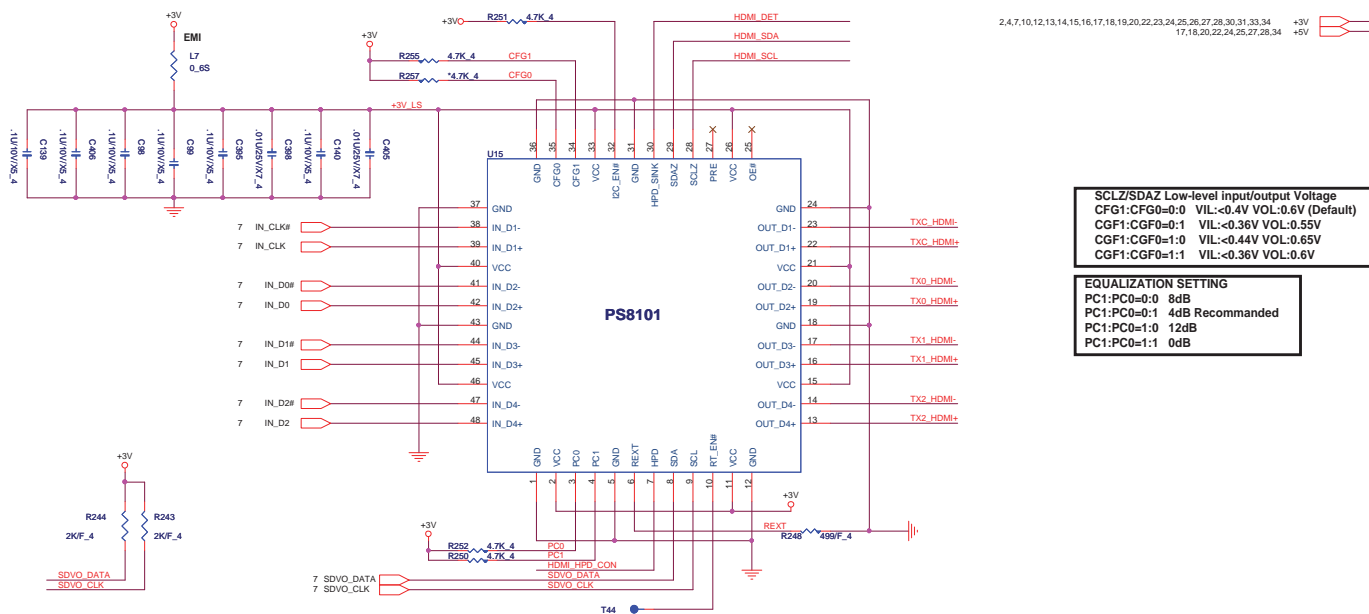


BACK LIGHT SUPPLY

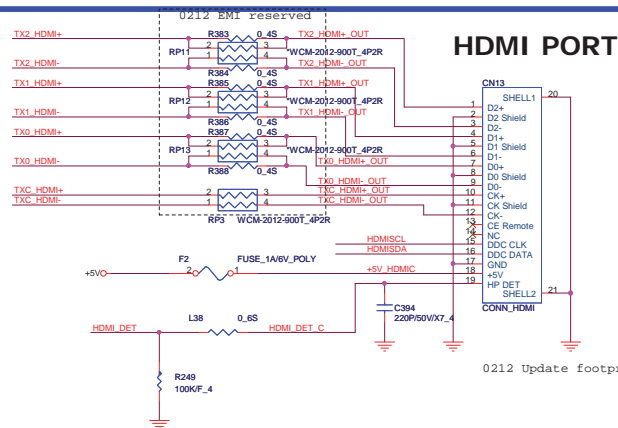
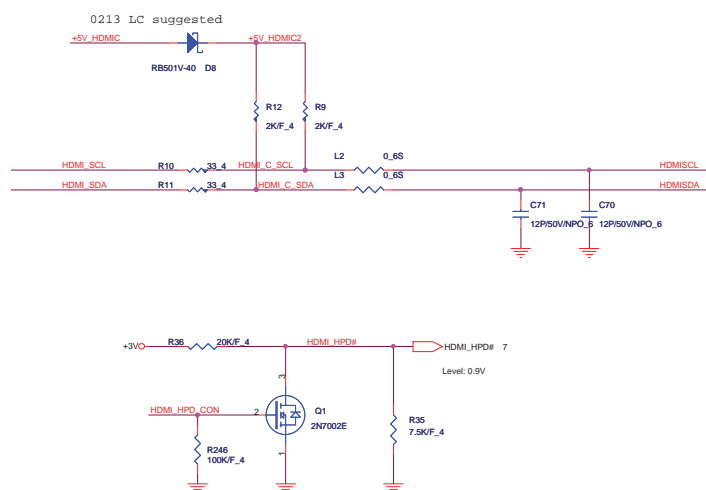


2,4,7,10,12,13,14,15,16,17,18,19,21,22,23,24,25,26,27,28,30,31,33,34 +3V
17,18,21,22,24,25,27,28,34 +5V
29,30,31,32,33,34 VIN
14,19,24,27,28,29,30,34 3VPCU

20



Reserve RP11-RP13 for EMI request Mika 20090422
 Remove RP4-RP6 and add R373-R375 Mika 20090320
 Change RP3 from 0ohm to WCM-2012-900T Mika 20090320

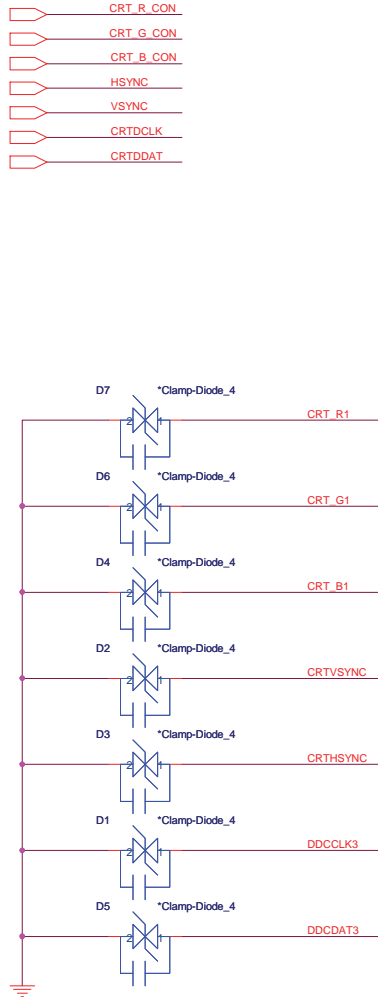


Swap CN5 Pin1,2,3,4,5 & Pin11,12,13,14,15 Mika 20090312
Change CN5 footprint Mika 20090318

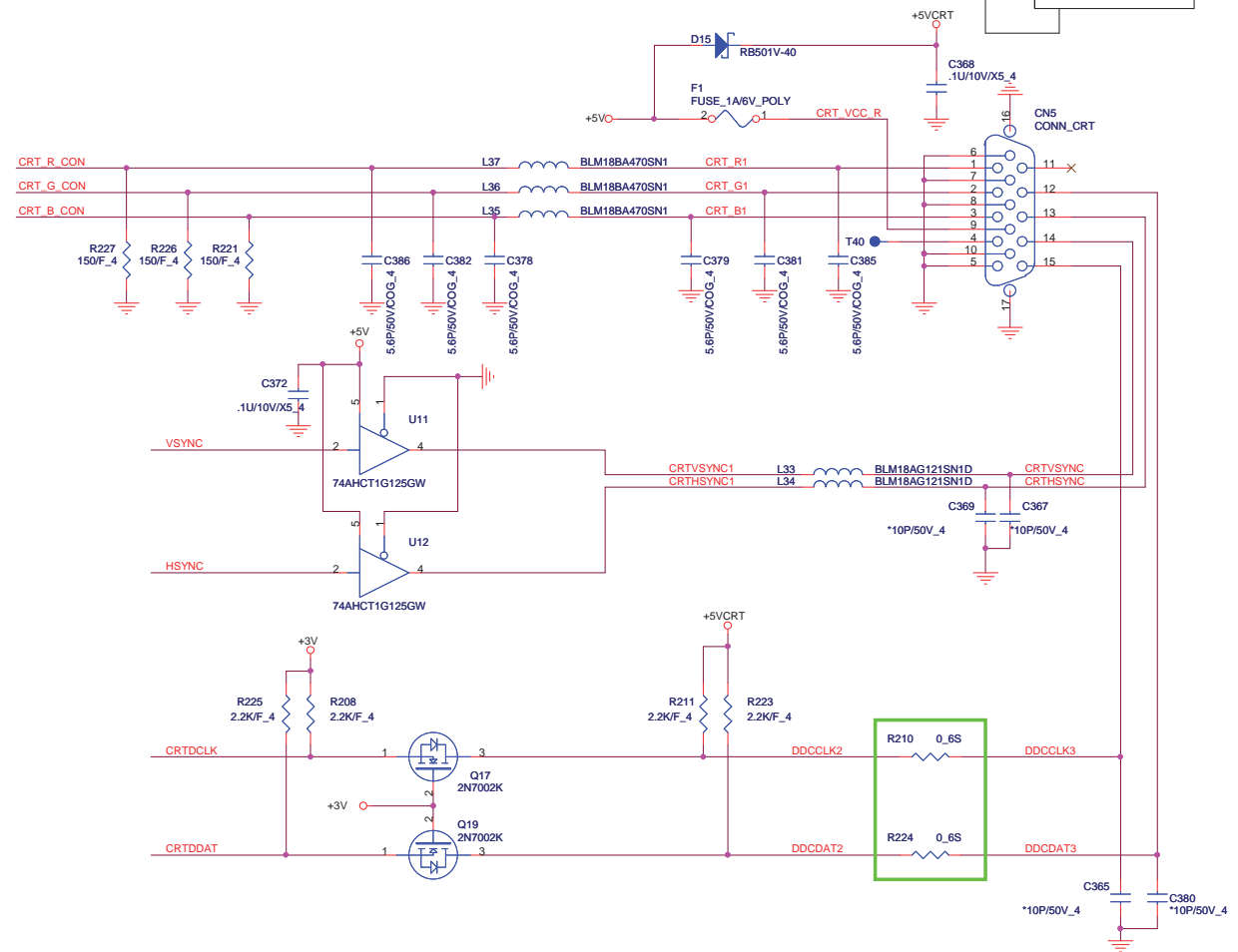
22

CRT PORT

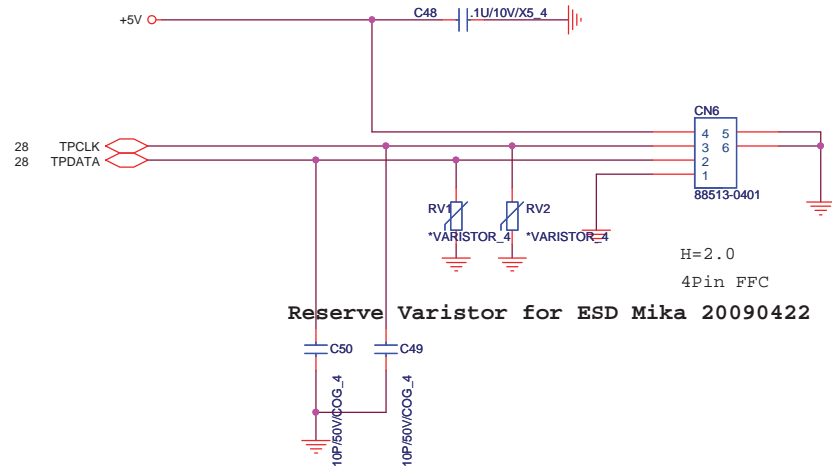
- 7 CRT_R_CON
- 7 CRT_G_CON
- 7 CRT_B_CON
- 7 HSYNC
- 7 VSYNC
- 7 CRTDCLK
- 7 CRTDDAT



0218 Change by ESD suggestion



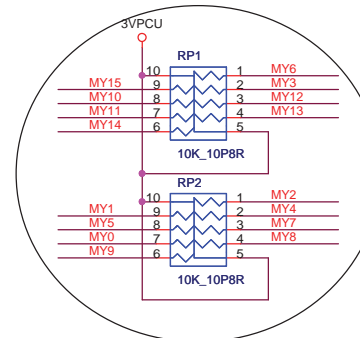
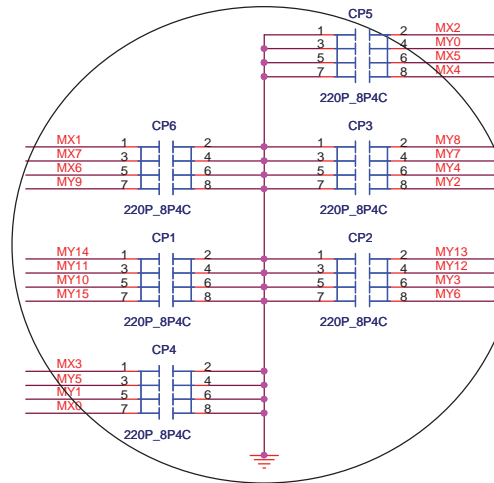
TOUCH PAD CONNECTOR



0212 Swap Pin definition
0216 Change TP conn. to 6P.

Change TP CONN to 4P Mika 20090305
Swap TP CONN Mika 20090312

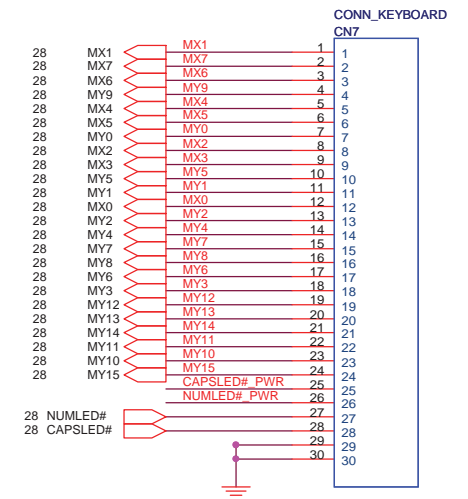
KEYBOARD CONNECTOR



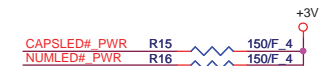
0223 Swap Keyboard Matrix for Routing

<-- Swap signal Mika 20090306

Swap pin definition Mika 20090305



0212 Swap Pin definition

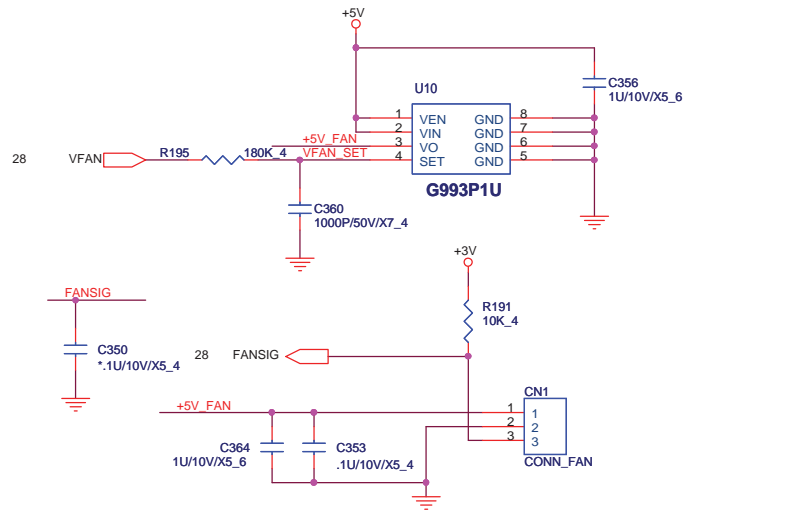


PROJECT :LL1
Quanta Computer Inc.

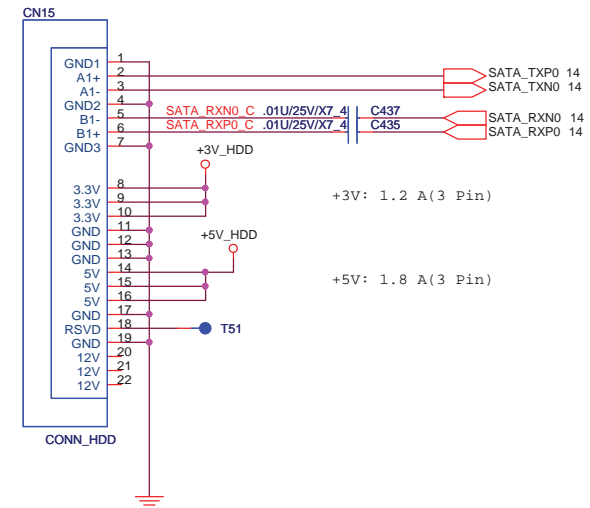
Size B Document Number <Doc> **CONN (KB, TP)** Rev 1A

Date: Thursday, April 23, 2009 Sheet 24 of 38

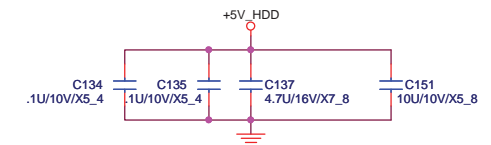
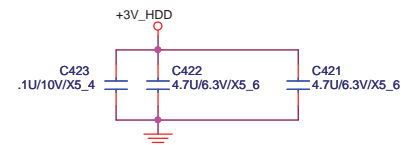
FAN CONTROL



SATA-HDD CONNECTOR



0213 Reserved for EMI, power consumption

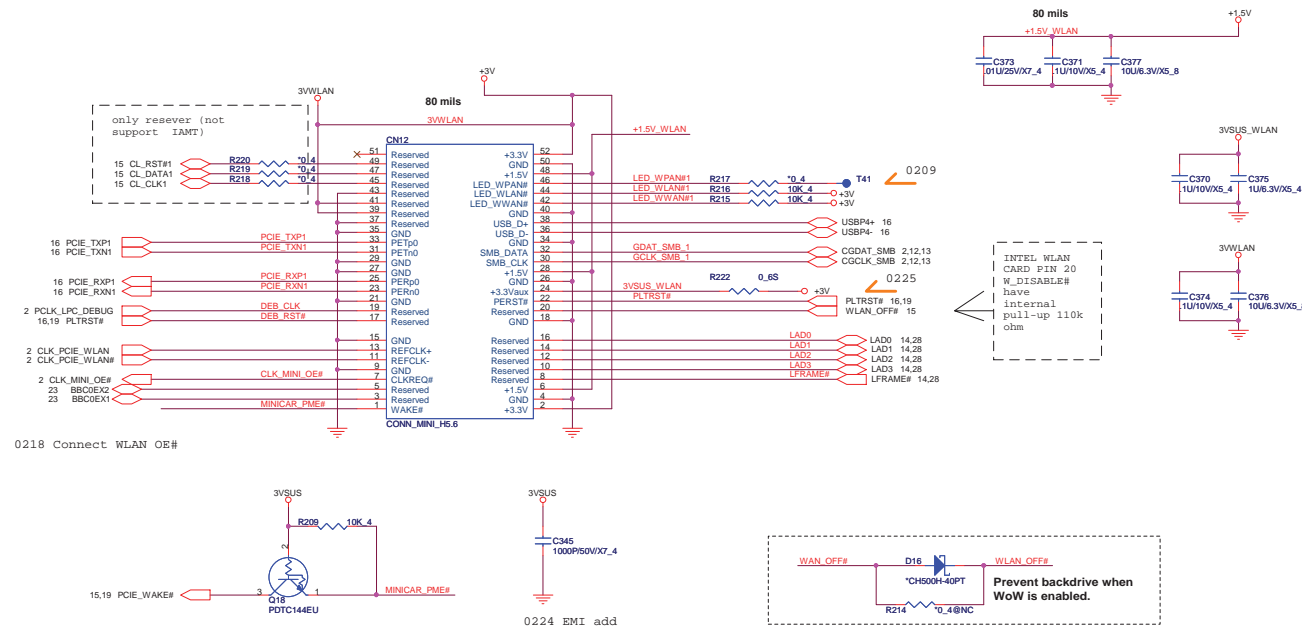


PROJECT :LL1
Quanta Computer Inc.

Size B	Document Number <Doc>	Rev 1A
CONN (HDD, FAN)		
Date: Thursday, April 23, 2009	Sheet 25 of 38	

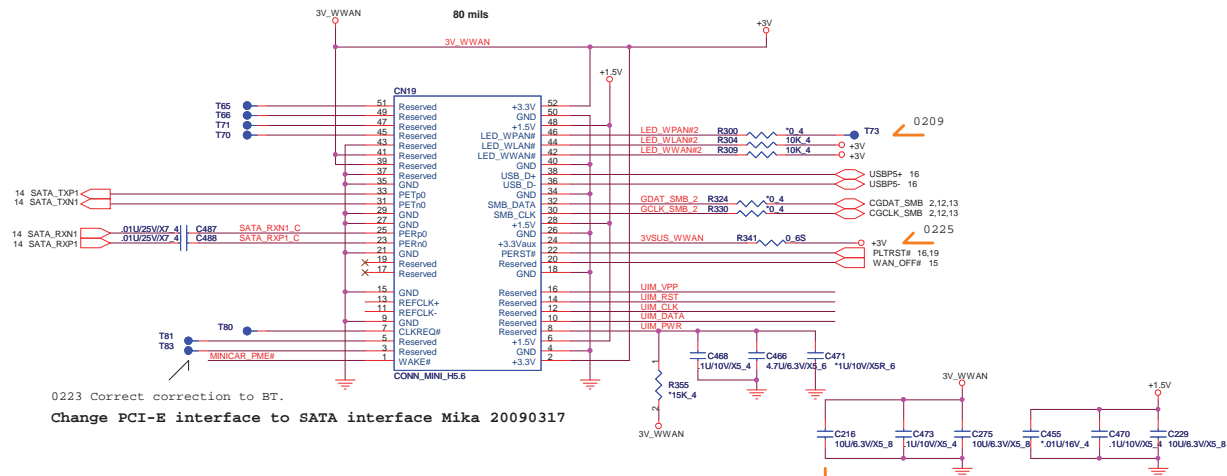
Mini PCI-E Card 1 WLAN

26

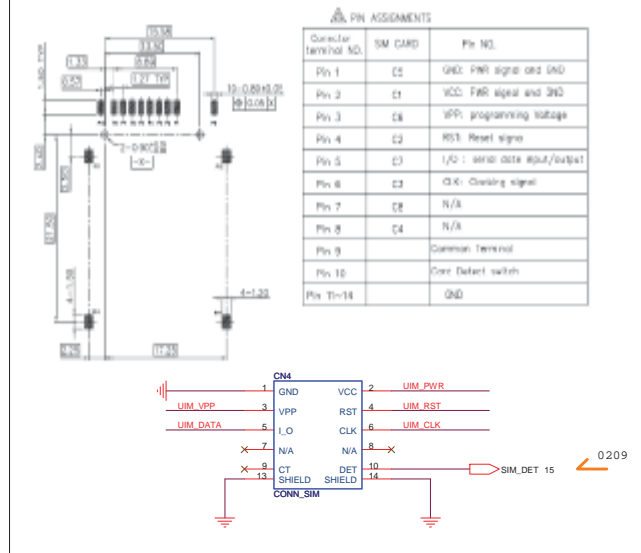


Mini PCI-E Card 2 WWAN(W/SIM)

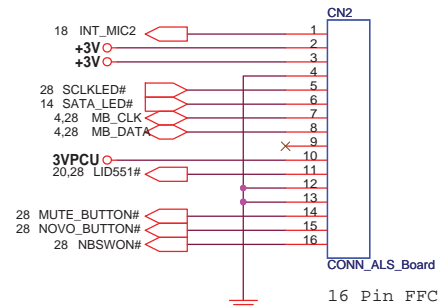
R222 and R341 Connect to +3V Mika 20090318



SIM SOCKET

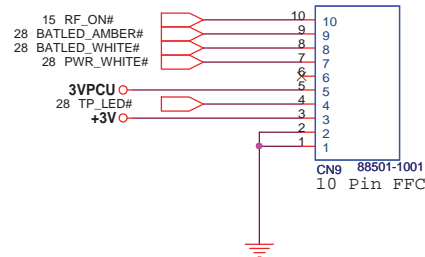


ALS/ Button Board



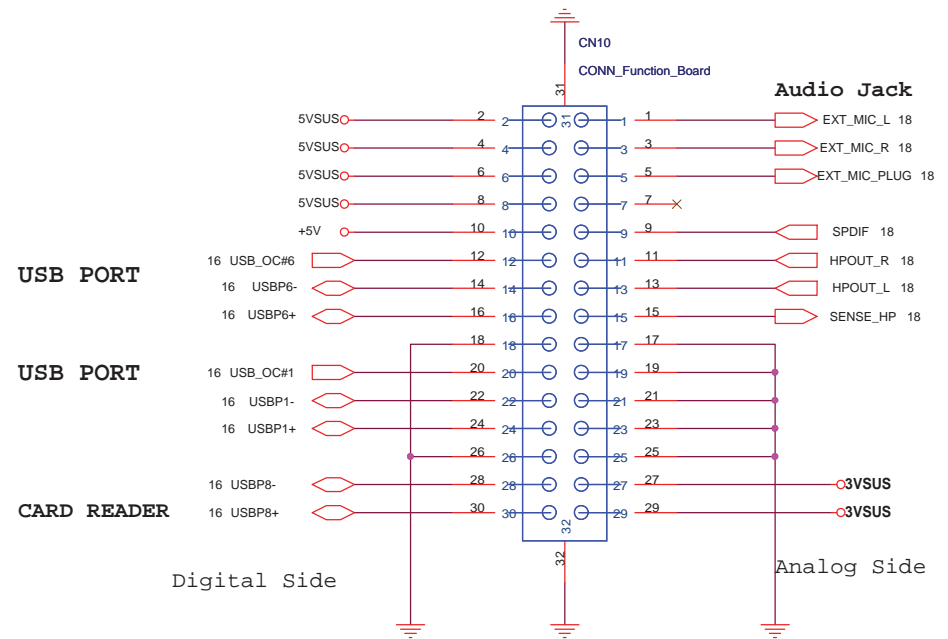
Change ALS smb to MB_CLK/MB_DATA Mika 20090421

Front LED indicator Board



Change Front LED CONN to 10P Mika 20090306

Function Board



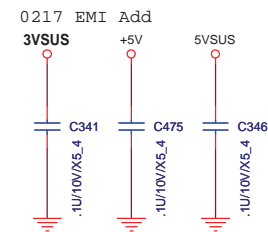
USB PORT


USB PORT

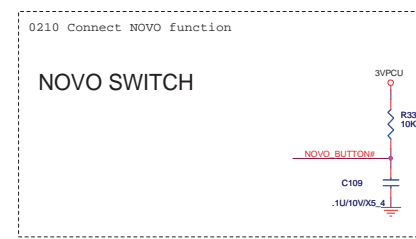
CARD READER

Digital Side

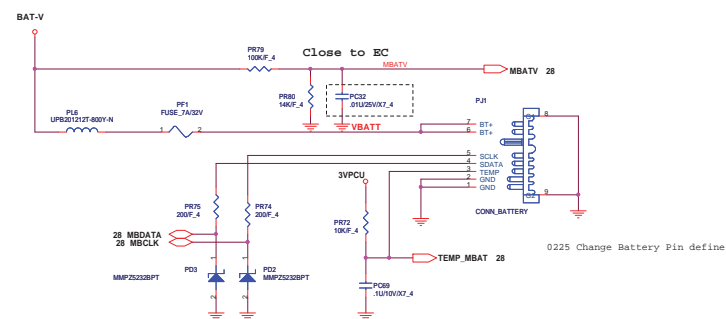
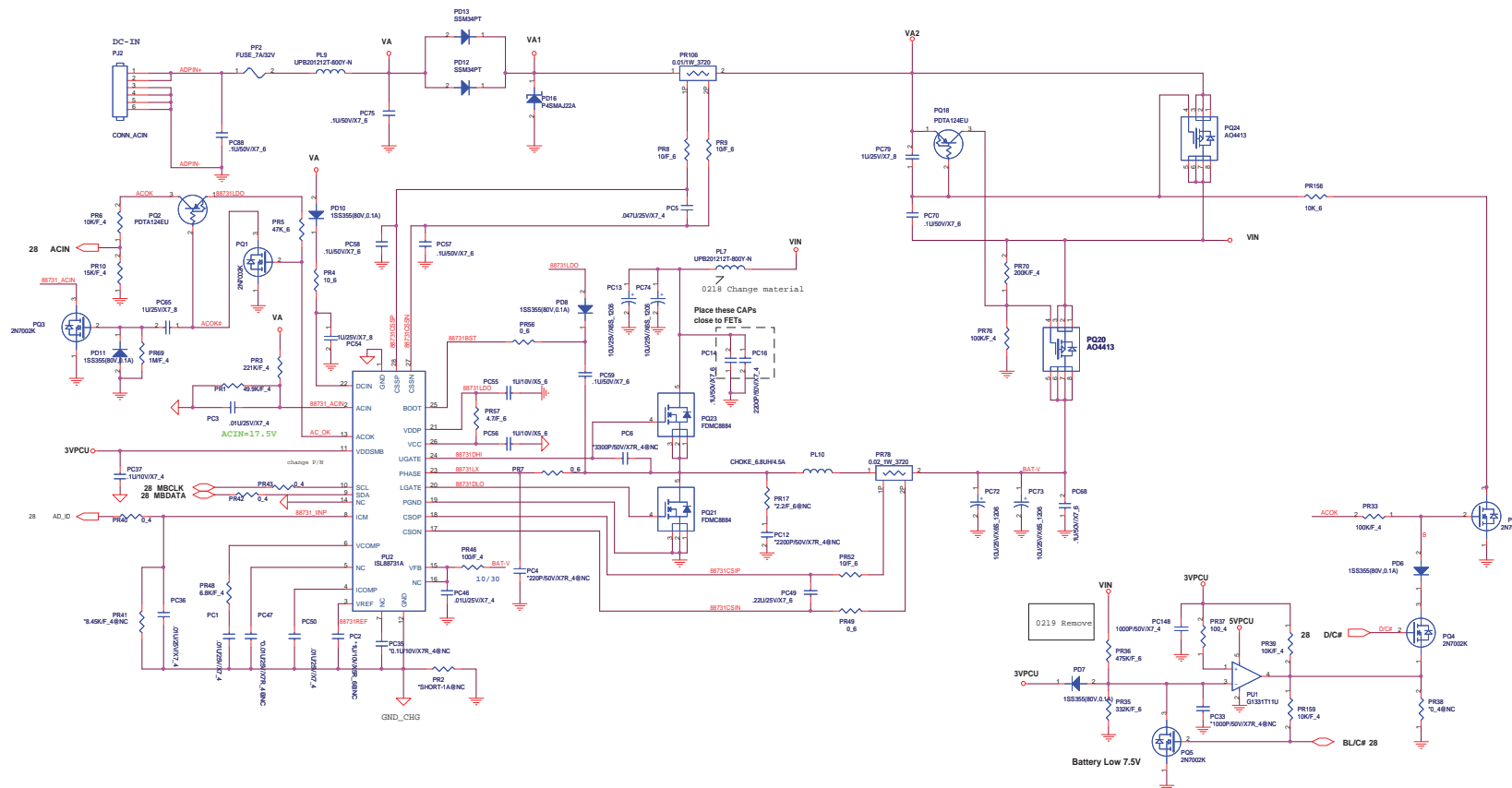
Analog Side



		PROJECT :LL1	
		Quanta Computer Inc.	
Size B	Document Number <Doc>	CONN (WIRE to BOARD, LED)	Rev 1A
Date:	Thursday, April 23, 2009	Sheet	27 of 38

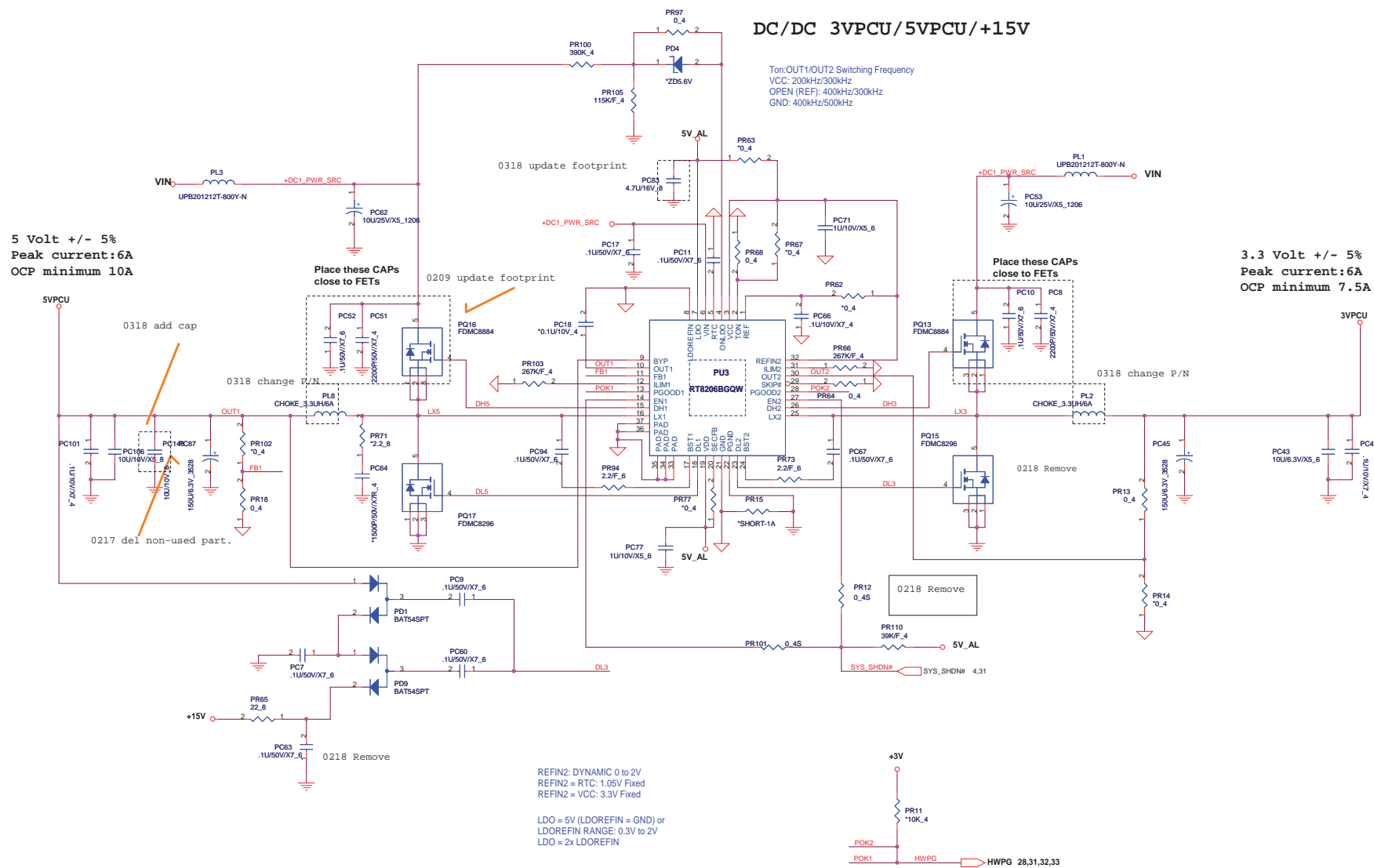


<http://hobi-elektronika.net>

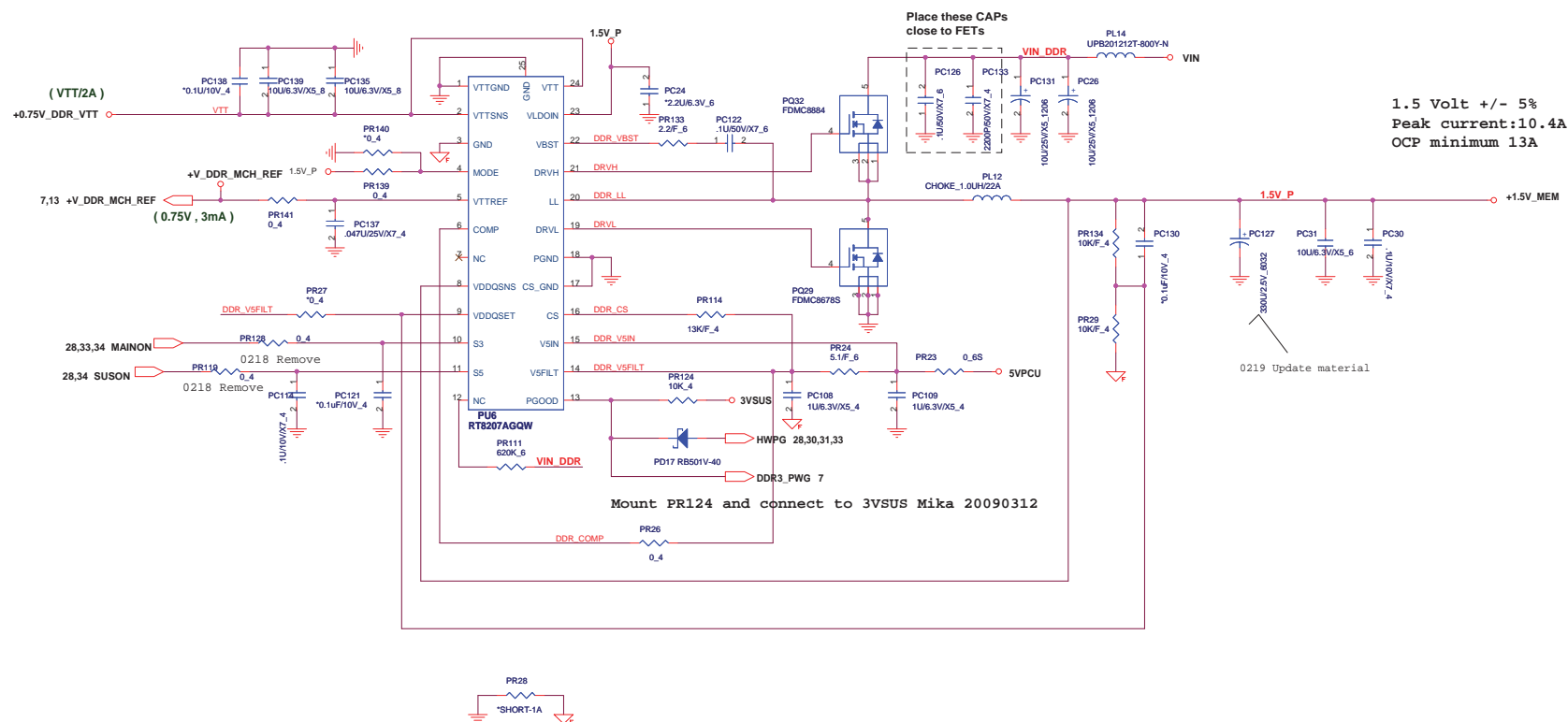


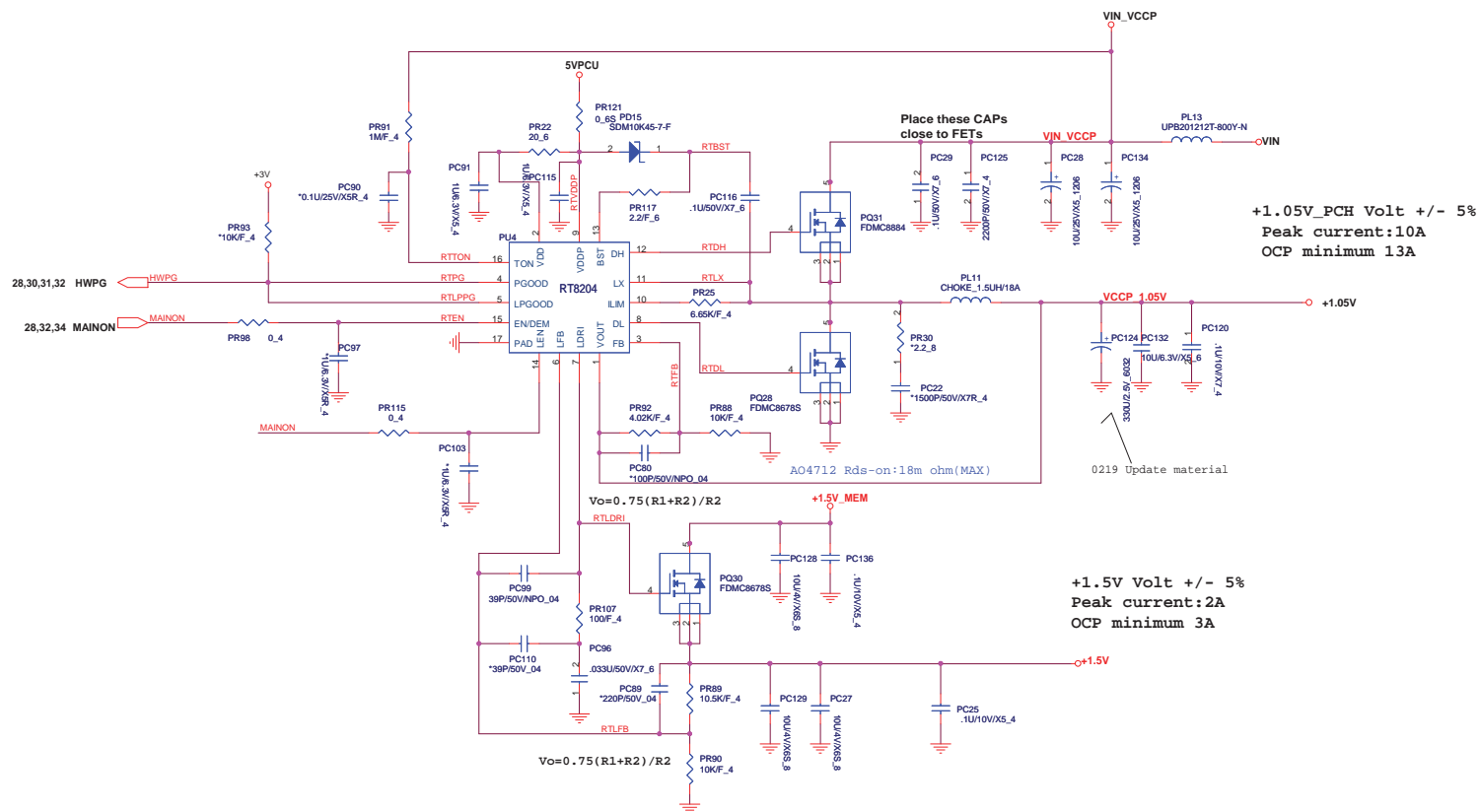
DC/DC 3VPCU/5VPCU/+15V

Ton:OUT1/OUT2 Switching Frequency
VCC: 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

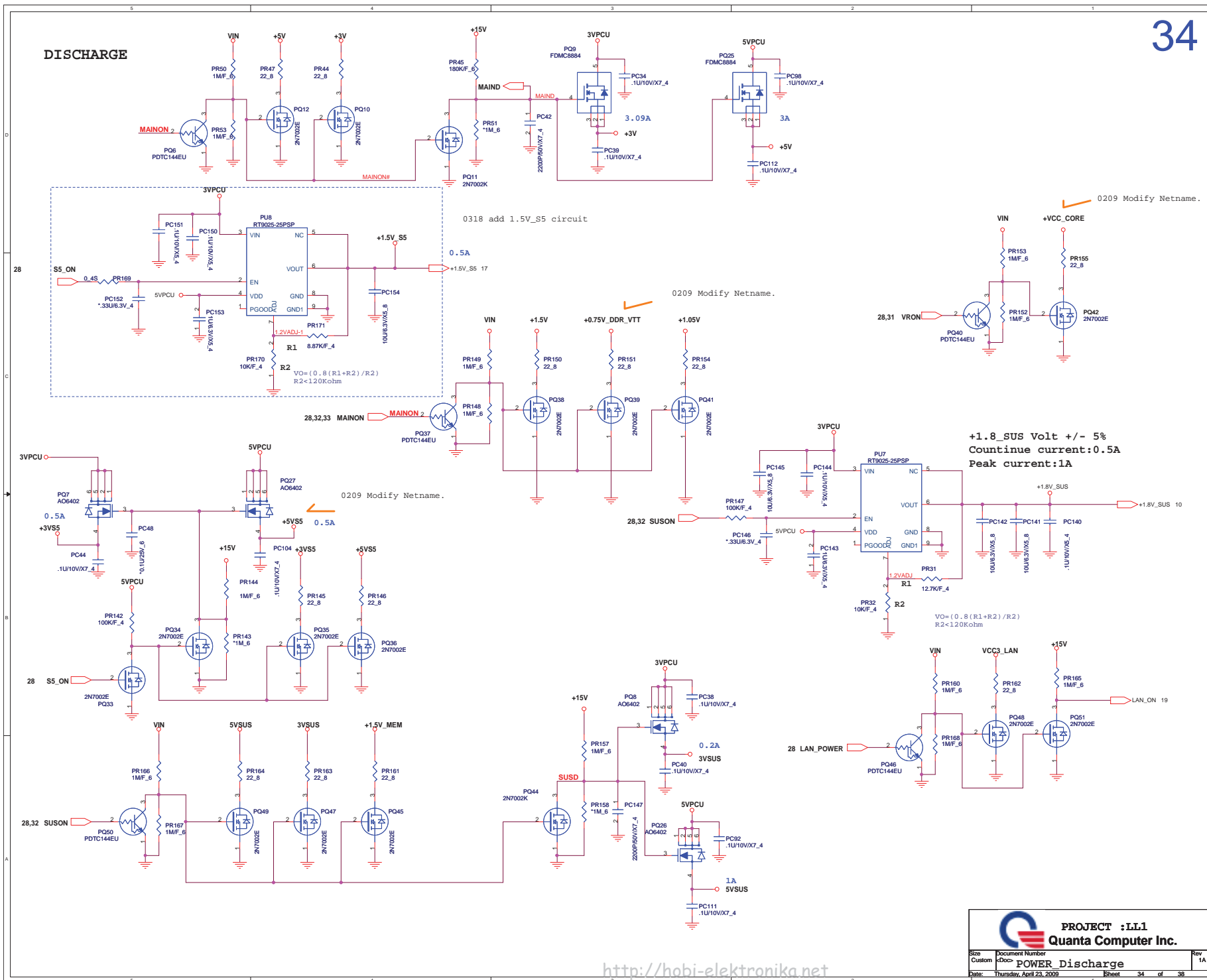


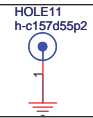
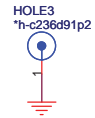




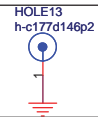


DISCHARGE

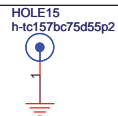
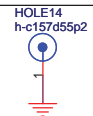




WLAN NUT



VGA NUT



WWAN NUT

Change Hole15 footprint Mika 20090316



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Quanta Computer Inc.

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02 -- Clock Generator
 1) Disable ITP...0211
 2) Connect VDD_IO to 1.05V...0216
 3) Connect WLAN PCI-E to SRC10 contrlled by CR#_H...0218
 4) Swap DREFFSSCLK pair to SRCCLK1 for spread spectrum...0220
 03 -- Penryn (HOST BUS) 1/3
 1) Del reserved ITP connector...0209
 2) Disconnect ITP Clock...0209
 3) Connect WLAN to SRC8, No clock request connect...0209
 4) Add PROCHOT# level shift between 1.05V and +3V...0211
 07 -- Cantiga_B (VGA,DMI)
 1) Connect DDR3 CH.A (CKE1,ODT1,CS1,M_CLK_DDR1) signals...0209
 2) Del SM_PWROK AND logic...0211
 3) Del PM_EXTTS#1 connection due to no DDR thermal monitor...0211
 4) Connect UMA HDA for HDMI support...0211
 5) Correct TV DAC disable connection...0218
 09 -- Cantiga_D (VCC,NCTF)
 1) Mount VCC_AXG_SENSE, VSS_AXG_SENSE 100hm...0209
 10 -- Cantiga_E (POWER)
 1) Add CRT DAC power to enable CRT feature...0211
 2) Add CRT Enable/ TV disable DAC power...0218
 12 -- DDR3 (A) SO-DIMM RVS
 1) Paste DDR3 socket module...0209
 2) Update DDR3 conn. footprint...0211
 3) Correct Dimm0 Address...0213
 13 -- DDR3 (B) SO-DIMM STD
 1) Del DDR thermal monitor...0209
 2) Update DDR3 conn. footprint...0211
 14 -- ICH9-M_A_(CPU,SATA,IDE)
 1) Connect HDA to UMA for iHDMI support...0211
 2) Correct SATA decoupling...0211
 16 -- ICH9-M_B_(USB,PCIE,DMI)
 1) Swap USB port for USB Host controller allocation...0219
 17 -- ICH9-M_D_(POWER,GND)
 1) Modfiy HDA BUS power plan to +1.5V(LC)...0213
 2) Add decoupling on VCCL1_05 as Design Guide request...0224
 18 -- AUDIO (CX20582, SPK)
 1) Correct PCBEEP (EC) netname...0209
 2) Update Conexant review result...0211
 3) Move MIC conn. to daugter board due to ME concern...0212
 4) Move Jack related components to daughter board...0213
 5) Correct Mute function...0213
 6) Modify MIC BIAS to net"AVDD_3.3V" (LC)...0213
 7) Modify HDA BUS power to +1.5V(LC)...0213
 8) Reserve PCBEEP Gain pull high for further experiment...0224.
 9) Del MIC-IN decoupling Cap. and change Pull High to 2.2K...0224
 10) Change MIC_IN VBIAS from Codec...0224.
 11) Enlarge +5VA trace width...0226
 19 -- LAN (BCM57780, RJ45)
 1) Update Transformer footprint...0209
 2) Update RJ45 footprint...0211
 3) Reserve 00hm short in LANVCC (LC)...0213
 4) Add 00hm short reserved for Energey_DET net(LC)...0213
 5) Change LAN Chip to BCM57780...0216
 6) Remove 1.6V single net...0216
 20 -- CONN (LVDS, CCD)
 1) Correct Backlight PWM netname from EC...0209
 2) Update LCD conn. footprint...0212
 3) Reserve LVDS +3V 00hm short for further experiment...0213
 4) Reserve CAMERA VCC 00hm short for further experiment...0213
 5) Reserve CCD USB port Common mode Choke...0217
 21 -- CONN (HDMI, level Shift)
 1) Add EMI reserved RP (0X2) in HDMI signals...0212
 2) Update HDMI conn. footprint...0212
 3) Add diode in +5V_HDMIC series(LC)...0213

22 -- CONN (CRT)
 1) Update CRT conn. footprint...0211
 2) Change ESD solution...0218
 23 -- CONN (USB, BT, G sensor)
 1) Update G-sensor footprint...0209
 2) Change USB port bulk from 100U to 150U(LC)...0213
 3) G-sensor follow HengshanII...0213
 4) Del additioanl USB power Bulk and filter...0218
 5) Correct BBCPEX1,2 connection...0223
 6) Swap USB net for routing...0224
 24 -- CONN (KB, TP)
 1) Update TP connector footprint...0209
 2) Swap TP pin definition...0212
 3) Swap KB pin definitoin...0212
 4) Swap Keyboard matrix for routing...0223
 25 -- CONN (HDD,FAN)
 1) Modify Fan connector and Pin define...0210
 2) Update HDD conn. footprint...0211
 3) Reserve HDD 3V/5V short jump for further EMI/power consumption check(LC)...0213
 4) Change FAN conn. to right angle...0217
 26 -- CONN (MINI PCI-E, SIM)
 1) Connect SIM socket Detect...0209
 2) Modify Mini Card LED indicator connection...0209
 3) Modify WWAN 470u bulk reserved to 10u...0211
 4) Connect WLAN OE#...0218
 5) Correct BBCPEX1,2 connection...0223
 6) EMI add 1000P filter in 3VSUS trace...0224
 7) Remove +3V to +3.3VAUX connection, reserve only 3VSUS...0225
 27 -- CONN (WIRE to BOARD, LED)
 1) Connect USB/Audio/CR function connector...0210
 2) Connect ALS/ Button connector...0210
 3) Connect Front LED indicator connector...0210
 4) Connecet MIC on ALS board...0212
 5) Update 30Pin Wire to Board conn. footprint...0212
 6) EMI add reserved filter for power trace...0217
 28 -- EC (ITE8502E)
 1) Connect NOVO function...0210
 2) NC un-used GPIO as test points...0210
 3) Connect G-sensor signals...0213
 4) Connect TP_LED#...0216
 5) Disconnect ENERGY_DET...0216

07 -- Cantiga_B (VGA,DMI)
 1) TV_DCONSEL_0/1 connect to GND ...0312
 2) Connect DDR3_PWG to NB ...0312
 3) Add R372 in ACZ_SDIN1 ...0317
 4) Add U22 and C486 for DDR3_PWG ...0318

14 -- ICH9-M_A_(CPU,SATA,IDE)
 1) Support PCI-E Type SSD ...0317
 2) PCI-E Type SSD change to SATA1 ...0320

15 -- ICH9-M_C_(PM,GPIO,SMB)
 1) Swap SIM_DET & CLK_SATA_OE# ...0312
 2) Connect SIM_DET to GPIO49 ...0317
 3) Connect SIM_DET to GPIO1 ...0319

16 -- ICH9-M_B_(USB,PCIE,DMI)
 1) Del PCI-E interface (WWAN use USB type) ...0317
 2) Change WLAN to PCI-E-2 ...0318

18 -- AUDIO (CX20582, SPK)
 1) Del R94,R163 to short AGND and GND directly ...0316
 2) Add C480 and C481 ...0316
 3) Change R344 to 1206 size ...0316
 4) Change C235 to 0.1U ...0316
 5) Change R166~R169 to 0603 size ...0316
 6) Del R156 and Q8 then short Volmute# directly ...0318
 7) Change PC_BEEP voltage level to 1/10 ...0319
 8)Change R166~R169 from 0ohm to BK1608HS601 ...0320

19 -- LAN (BCM57780, RJ45)
 1) Change LAN CONN footprint ...0305
 2) Connect LOM_DISABLE# to EC ...0310
 3) Swap U9 pin5 pin6 ...0312

21 -- CONN (HDMI, level Shift)
 1) Remove RP4~RP6 and add R373~R375 ...0320
 2) Change RP3 from 0ohm to WCM-2012-900T ...0320

22 -- CONN (CRT)
 1) Swap CN5 Pin1,2,3,4,5 & Pin11,12,13,14,15 ...0312
 2) Change CN5 footprint ...0318

23 -- CONN (USB, BT, G sensor)
 1) Change USB CONN footprint ...0305
 1) Change USB CONN footprint ...0318

24 -- CONN (KB, TP)
 1) Swap CN7 pin definition ...0305
 2) Change TP conn to 4P ...0305
 3) Swap KB bypass capacity and resistor ...0306
 4) Swap TP CONN ...0312

26 -- CONN (MINI PCI-E, SIM)
 1) Change PCI-E interface to SATA interface ...0317
 2) R222 and R341 Connect to +3V ...0318

27 -- CONN (WIRE to BOARD, LED)
 1) Change Front LED CONN to 10P ...0306

28 -- EC (ITE8502E)
 1) Swap Y3 PIN1 and PIN4 ...0319

31 -- POWER_CPU CORE (RT8152B)
 1) PR123 change to 499ohm ...0317
 2) Del PR120 and PR131 ...0317

32 -- POWER_DDR3 (RT8207AGQW)
 1) Mount PR124 and connect to 3VSUS ...0312

35 -- HOLES, PAD, NUT
 1) Change Hole15 footprint ...0316

14 -- ICH9-M_A_(CPU,SATA,IDE)
1) Add charge schematic for RTC ...0421

18 -- AUDIO (CX20582, SPK)
1) Change PC_BEEP voltage level to 2/3 ...0421
2) By vendor suggestion "D22 and D23 close to codec" ...0421

21 -- CONN (HDMI, level Shift)
1) Reserve RP11~RP13 for EMI request ...0422

23 -- CONN (USB, BT, G sensor)
1) Increase Z-axis signal ...0415

24 -- CONN (KB, TP)
1) Reserve Varistor for ESD ...0422

27 -- CONN (WIRE to BOARD, LED)
1) Change ALS smb to MB_CLK/MB_DATA ...0421

28 -- EC (ITE8502E)
1) Change ID_PIN to pull high ...0421
2) Reserve capacity on LED signal for EMI ...0421

change 0 Ohm to short footprint:

P02: (1) Short connect R99.

P10: (1) Short connect R45, R57

P20: (1) Short connect R3, R4

P21: (1) Short connect L2, L3, L38

P22: (1) Short connect R210, R224

P23: (1) Short connect R111, R281, R283

P28: (1) Short connect R79, R274

P30: (1) Short connect PR12, PR101

P31: (1) Short connect PR82, PR83, PR87, PR96, PR99 PR104, PR108, PR113, PR135

P32: (1) Short connect PR23

P33: (1) Short connect PR121

P34: (1) Short connect PR169